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Chang Rock SONG	)	Confirmation No. 7126
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Application No. 09/982,023	)	Group Art Unit: 2823
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Filed: October 19, 2001	)	Examiner: S. Foong
	)	
For: METHOD OF MANUFACTURING A CAPACITOR IN A SEMICONDUCTOR DEVICE	)	Mail Stop Non-Fee Amendment
	)	

Translation

6/18/03

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Crystal Plaza Two, Lobby, Room 1B03
Arlington, VA 22202

Sir:

VERIFICATION OF TRANSLATION

I, the below named translator, hereby declare that:

My name and post office address are as stated below.

That I am knowledgeable in the English language and in the Korean language and believe the attached English translation to be a true and complete translation of the below identified document.

The document for which the attached English translation is being submitted is the Korean Patent Application No. 2000-62025 filed in Korea on October 20, 2000. This Korean language document was filed in the U.S. Patent and Trademark Office on October 19, 2001.

I hereby declare that all statements made herein of my knowledge and true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issue thereon.

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Signature of the translator: Jin Seok Kim

Date: June 10, 2003

[ABSTRACT]

[Summary]

A method of manufacturing a capacitor in semiconductor devices comprises a first step of depositing an oxide in order to insulate a silicon substrate and a capacitor on the entire surface of the substrate and forming a nitride having an high etch selectivity to the oxide; a second step of forming a contact hole for a vertical wiring between the substrate and the capacitor; a third step of depositing a polycrystal doped Si on the entire surface while filling the contact hole; a fourth step of removing a portion of the polycrystal doped Si within the contact hole while removing the polycrystal doped Si on the entire surface except for the contact hole; a fifth step of depositing Ti or Co on the entire surface, performing a thermal process to form a titanium silicide or a cobalt silicide on an upper side of the polycrystal doped Si within the contact hole and removing remaining Ti or Co; a sixth step of depositing an anti-diffusion film (TiN or TiAlN) on the entire surface while filling the contact hole; a seventh step of flattening TiN or TiAlN on the substrate while completely removing TiN or TiAlN; a eighth step of depositing a silicate glass on the entire surface; a ninth step of forming a hole for forming a capacitor in the silicate glass right on the contact hole; a tenth step of depositing a Ru electrode on the entire surface; a eleventh step of removing the Ru electrode on the silicate; a twelfth step of processing the Ru electrode by means of NH_3-plasma process; a thirteenth step of performing a N_2O-plasma process; a fourteenth step of depositing a BST dielectric thin film on the entire surface; a fifteenth step of processing the BST dielectric thin film by means of a rapid thermal process in order to crystallize the BST dielectric thin film; a sixteenth step of depositing an upper electrode on the entire surface; and a seventh step of performing the entire capacitor structure in order to stabilize the entire structure.

[Representative Drawing]

Fig. 14

[Index Word]

Capacitor, Ru electrode

[SPECIFICATION]

[Title of the Invention]

METHOD OF MANUFACTURING CAPACITOR IN SEMICONDUCTOR DEVICES

[Brief Description of the Drawings]

Figs. 1 through 14 are schematic diagrams for explaining a method of manufacturing a capacitor n semiconductor devices according to the present invention.

<the Reference Numerals in the Drawings>

1: silicon substrate	6: anti-diffusion film
2: silicon oxide	7: silicate glass
3: nitride	8: underlying electrode Ru
4: doped polycrystal Si	9: BST dielectric film
5: ohmic contact layer	10: upper electrode Ru

[Detailed Description of the Invention]

[Object of the Invention]

[Technological Background of the Invention and Description of the Prior Art]

The invention relates generally to a method of manufacturing a capacitor in semiconductor devices, and more particularly to, a method o f m anufacturing a c apacitor i n semiconductor devices capable of preventing defective Ru/BST/Ru capacitors By depositing an underlying electrode (Ru) by means of chemical vapor deposition method and then stabilizing the surface of the underlying electrode (Ru) by a given thermal process in a process of manufacturing a capacitor in a DRAM device having the integration degree of over 1Gbit.

Currently, there is a trend that Ta_2O_5 or BST is increasingly used as a dielectric thin film used in a DRAM in a $SiO_2/Si_3N_4/SiO_2$ stack structure. In the near future, it is expected that BST will be the most promising dielectric thin film in a design rule applied in over 1Gbit. This dielectric thin film is formed on a patterned substrate by means of a chemical vapor deposition method if being applied to an actual device having a fine design rule. In

case that today's BST is used as a dielectric thin film, it is expected that a concave type Ru/BST/Ru capacitor and a stack type Pt/BST/Pt capacitor are the most promising candidates. In case of Pt used as an electrode material, it shows a very stable capacitor characteristic without regard to its formation method or a post-process due to it very stable interface characteristic with BST. On the other hand, in case of Ru, it does not show a still stable capacitor characteristic since it degrades the quality of BST when BST is deposited due to its easily oxidized characteristic and its low catalyst characteristic compared to Pt. In summary, Pt allows a very good BST film quality when BST is deposited by means of a chemical vapor deposition method since Pt contains a lot of very activated oxygen atoms due to its catalytic characteristic. However, Ru degrades the BST film quality since Ru has a trend that it forms a RuO_2 oxidization phase instead of activated oxygen atoms without silver catalyst characteristic.

Furthermore, in case of Ru, it must be processed at a very low temperature(250□270□) in order to deposit Ru by means of chemical vapor deposition method while prohibiting creating of RuO_2. Due to this, Ru affects a BST thin film or an underlying anti-diffusion film since it contains a lot of carbon and oxygen during a subsequent process. Even in view of a flat dimension, there are few that a good BST characteristic deposited on Ru by means of a chemical vapor deposition method can be obtained. Thus, there are facts that development of a concave type Ru/BST/Ru capacitor is delayed. Most researches so far include at most performing a rapid thermal process (RTP) under nitrogen or argon atmosphere in order to fine a Ru film. Therefore, there is a need for a process of changing a Ru surface characteristic in order to improve an interfacial characteristic of BST/Ru.

[Technical Means for Achieving the Object of the Invention]

It is therefore an object of the present invention to provide a method of manufacturing a capacitor in semiconductor devices capable of preventing defective Ru/BST/Ru capacitors by depositing an underlying electrode (Ru) by means of chemical vapor deposition method and then stabilizing the surface of the underlying electrode (Ru) by a given thermal process.

According to the present invention, a BST/Ru interface characterizing in a low leakage current as well as a dielectric constant can be obtained to improve reliability of a

capacitor.

[Structure and Operation of the Invention]

In order to accomplish the above object, a method of manufacturing a capacitor in semiconductor devices according to the present invention, is characterized in that it comprises a first step of depositing an oxide in order to insulate a silicon substrate and a capacitor on the entire surface of the substrate and forming a nitride having an high etch selectivity to the oxide; a second step of forming a contact hole for a vertical wiring between the substrate and the capacitor; a third step of depositing a polycrystal doped Si on the entire surface while filling the contact hole; a fourth step of removing a portion of the polycrystal doped Si within the contact hole while removing the polycrystal doped Si on the entire surface except for the contact hole; a fifth step of depositing Ti or Co on the entire surface, performing a thermal process to form a titanium silicide or a cobalt silicide on an upper side of the polycrystal doped Si within the contact hole and removing remaining Ti or Co; a sixth step of depositing an anti-diffusion film (TiN or TiAlN) on the entire surface while filling the contact hole; a seventh step of flattening TiN or TiAlN on the substrate while completely removing TiN or TiAlN; a eighth step of depositing a silicate glass on the entire surface; a ninth step of forming a hole for forming a capacitor in the silicate glass right on the contact hole; a tenth step of depositing a Ru electrode on the entire surface; a eleventh step of removing the Ru electrode on the silicate; a twelfth step of processing the Ru electrode by means of NH_3-plasma process; a thirteenth step of performing a N_2O-plasma process; a fourteenth step of depositing a BST dielectric thin film on the entire surface; a fifteenth step of processing the BST dielectric thin film by means of a rapid thermal process in order to crystallize the BST dielectric thin film; a sixteenth step of depositing an upper electrode on the entire surface; and a seventh step of performing the entire capacitor structure in order to stabilize the entire structure.

In order to fill the contact hole in the third step, a polycrystal doped Si is deposited in thickness of 700□3000□ by means of a chemical vapor deposition method.

The polycrystal doped Si within the contact hole in the fourth step is removed by 200□1500□ from the top.

The titanium silicide and the cobalt silicide is the fifth step are formed in thickness of

100-500□.

TiN or TiAiN is used as the anti-diffusion film in the sixth step and is deposited in thickness of 700-3000□ by physical vapor deposition method or chemical vapor deposition method.

USG or PSG is used as the silicate glass in the eighth step and is formed in thickness of 2000-15000□.

The underlying electrode Ru is the tenth step is deposited in thickness of 100-500□ by means of sputtering method or chemical vapor deposition method on the basis of a sidewall.

The NH_3-plasma process in the twelfth step is performed under the conditions that the power is 100-500W, the pressure is 0.5-2.0Torr, the flow rate of NH_3 is 200-2000sccm and the temperature is 350-700□.

The N_2O-plasma process in the thirteenth step is performed under the conditions that the power is 100-500W, the pressure is 0.5-2.0Torr, the flow rate of N_2O is 200-2000sccm and the temperature is 350-700□.

The BST dielectric film in the fourteenth step is deposited in thickness of 150-500□ by means of chemical vapor deposition method.

The BST dielectric thin film in the fifteenth step is experienced by a thermal treatment using a mixture gas of oxygen and nitrogen or oxygen and argon at the temperature of 500-750□ for 10-180 seconds in order to crystallize the dielectric thin film.

The upper electrode Ru, Ir or Pt in the sixteenth step is deposited in thickness of 150-500□ by sputtering method or chemical vapor deposition method on the basis of a sidewall.

In order to stabilize the entire capacitor structure in the seventh step, the capacitor structure is experienced by a thermal treatment using a mixture gas of oxygen and nitrogen or oxygen and argon at the temperature of 400-800□ for 1-130 minutes.

The present invention will be described in detail by way of a preferred embodiment with reference to accompanying drawings, in which like reference numerals are used to identify the same or similar parts.

In order to overcome conventional problems, conditions that must be accomplished in a post-processing of a Ru thin film include: 1) fineness of a thin film, 2) reduction in the surface roughness and 3) adsorption of activated oxygen on the surface of Ru. For the purpose of this, the present invention forms an underlying electrode Ru on a patterned wafer

and then performs a two-step plasma treatment by which a NH_3-plasma process is performed in order to reduce the surface roughness and N_2O-plasma process is performed in order to adsorb the activated oxygen.

Fig. 1 shows a result of comparing the surface roughness in the case that a Ru thin film deposited by a dc-sputtering method is experienced by a rapid thermal process at the temperature of 600□ under nitrogen atmosphere and the case that the Ru thin film is experienced by NH_3-plasma process at the temperature of 600□. It can be seen from Fig. 1 that the case of NH_3-plasma process is further smaller than the case of a rapid thermal process in the root-mean-square (Rms) value representing the surface. The Rms value in the case of the NH_3-plasma process is further small even with being deposited. Therefore, the NH_3-plasma process not only fines the Ru thin film but also improve the surface roughness.

Fig. 2 shows the surface roughness of the Ru surface in the case that Ru is experienced by N_2O-plasma process at the temperature of 350□, Fig. 3 shows a result of XRD of the Ru surface and Fig. 4 represents a diffusion curve of oxygen atoms. As can be seen from Fig. 2, if N_2O-plasma process is applied, the surface roughness is a little increased but as can be seen from Fig. 3, a RuO_2 phase preventing BST from being deposited by means of a chemical vapor deposition method is not generated so that a lot of oxygen can be adsorbed on the surface of Ru, as can be seen from Fig. 4. The activated oxygen atoms improves the quality of a BST thin film firstly deposited on the Ru surface when BST is deposited by means of a chemical vapor deposition method so that a good BST/Ru interface characteristic can be obtained.

As shown in Fig. 5, a silicon oxide (2) of an insulating material is formed on the entire surface of a silicon substrate (1) in which semiconductor circuits are formed. A nitride (3) having a good etch selectivity to an oxide is formed in thickness of 300□1000□. Next, a contact hole is formed on a given portion of the insulating in which a capacitor will be formed and the nitride film, for a vertical wiring between an underlying substrate (1) and a capacitor. Then, as shown in Fig. 6, a doped polycrystal Si (4) is deposited on the entire surface of the substrate by chemical vapor deposition method while filling the contact hole. Etch-back process is performed to remove a portion of Si on an upper side of the contact hole, as shown in Fig. 7. As shown in Fig. 8, an ohmic contact layer (5) is formed on Si within the contact hole. Then, after forming a nitride for an anti-diffusion film (6) is formed on the

resulting surface, as shown in Fig. 9, the remaining nitride except for the nitride within the contact hole is removed by means of chemical mechanical polishing method, as shown in Fig. 10. Next, a silicate glass (7) is formed on the entire surface, as shown in Fig. 11, and a concave hole is formed by means of etching process. As shown in Fig. 12, after depositing an underlying electrode Ru (8) on the entire surface by means of a sputtering method or a chemical vapor deposition method, Ru of the entire surface except for Ru on the internal wall of the hole is removed by means of chemical mechanical polishing method or etch-back process, as shown in Fig. 13. After sequentially performing a NH_3-plasma + N_2O-plasma, as shown in Fig. 14, BST is deposited by means of chemical vapor deposition method and an upper electrode (10) is then formed to complete a capacitor.

[Effect of the Invention]

As can be understood from the above description with the present invention, the two-step plasma treatment method according to the present invention sequentially performs NH_3-plasma process+ N_2O plasma process + BST deposition, when BST is deposited by means of a chemical vapor deposition method. Therefore, the present invention can not only improve the quality of a BST thin film but also increase the efficiency of the equipment.

[CLAIMS]

[Claim 1]

A method of manufacturing a capacitor in semiconductor devices, comprising:

a first step of depositing an oxide in order to insulate a silicon substrate and a capacitor on the entire surface of the substrate and forming a nitride having an high etch selectivity to the oxide;

a second step of forming a contact hole for a vertical wiring between said substrate and said capacitor;

a third step of depositing a polycrystal doped Si on the entire surface while filling said contact hole;

a fourth step of removing a portion of said polycrystal doped Si within said contact hole while removing said polycrystal doped Si on the entire surface except for said contact hole;

a fifth step of depositing Ti or Co on the entire surface, performing a thermal process to form a titanium silicide or a cobalt silicide on an upper side of said polycrystal doped Si within said contact hole and removing remaining Ti or Co;

a sixth step of depositing an anti-diffusion film (TiN or TiAlN) on the entire surface while filling said contact hole;

a seventh step of flattening TiN or TiAlN on the substrate while completely removing TiN or TiAlN;

a eighth step of depositing a silicate glass on the entire surface;

a ninth step of forming a hole for forming a capacitor in the silicate glass right on said contact hole;

a tenth step of depositing a Ru electrode on the entire surface;

a eleventh step of removing said Ru electrode on said silicate;

a twelfth step of processing said Ru electrode by means of NH_3-plasma process;

a thirteenth step of performing a N_2O-plasma process;

a fourteenth step of depositing a BST dielectric thin film on the entire surface;

a fifteenth step of processing said BST dielectric thin film by means of a rapid thermal process in order to crystallize said BST dielectric thin film;

a sixteenth step of depositing an upper electrode on the entire surface; and

a seventh step of performing the entire capacitor structure in order to stabilize the entire structure.

[Claim 2]

The method of manufacturing a capacitor in semiconductor devices according to claim 1, wherein in order to fill said contact hole in said third step, a polycrystal doped Si is deposited in thickness of 700□3000□ by means of a chemical vapor deposition method.

[Claim 3]

The method of manufacturing a capacitor in semiconductor devices according to claim 1, wherein the polycrystal doped Si within said contact hole in said fourth step is removed by 200□1500□ from the top.

[Claim 4]

The method of manufacturing a capacitor in semiconductor devices according to claim 1, wherein said titanium silicide and said cobalt silicide is said fifth step are formed in thickness of 100-500□.

[Claim 5]

The method of manufacturing a capacitor in semiconductor devices according to claim 1, wherein TiN or TiAiN is used as said anti-diffusion film in said sixth step and is deposited in thickness of 700-3000□ by physical vapor deposition method or chemical vapor deposition method.

[Claim 6]

The method of manufacturing a capacitor in semiconductor devices according to claim 1, wherein USG or PSG is used as said silicate glass in said eighth step and is formed in thickness of 2000-15000□.

[Claim 7]

The method of manufacturing a capacitor in semiconductor devices according to

claim 1, wherein said underlying electrode Ru is said tenth step is deposited in thickness of 100-500□ by means of sputtering method or chemical vapor deposition method on the basis of a sidewall.

[Claim 8]

The method of manufacturing a capacitor in semiconductor devices according to claim 1, wherein said NH_3-plasma process in said twelfth step is performed under the conditions that the power is 100-500W, the pressure is 0.5-2.0Torr, the flow rate of NH_3 is 200-2000sccm and the temperature is 350-700□.

[Claim 9]

The method of manufacturing a capacitor in semiconductor devices according to claim 1, wherein said N_2O-plasma process in said thirteenth step is performed under the conditions that the power is 100-500W, the pressure is 0.5-2.0Torr, the flow rate of N_2O is 200-2000sccm and the temperature is 350-700□.

[Claim 10]

The method of manufacturing a capacitor in semiconductor devices according to claim 1, wherein said BST dielectric film in said fourteenth step is deposited in thickness of 150-500□ by means of chemical vapor deposition method.

[Claim 11]

The method of manufacturing a capacitor in semiconductor devices according to claim 1, wherein said BST dielectric thin film in said fifteenth step is experienced by a thermal treatment using a mixture gas of oxygen and nitrogen or oxygen and argon at the temperature of 500-750□ for 10-180 seconds in order to crystallize said dielectric thin film.

[Claim 12]

The method of manufacturing a capacitor in semiconductor devices according to claim 1, wherein the upper electrode Ru, Ir or Pt in said sixteenth step is deposited in thickness of 150-500□ by sputtering method or chemical vapor deposition method on the

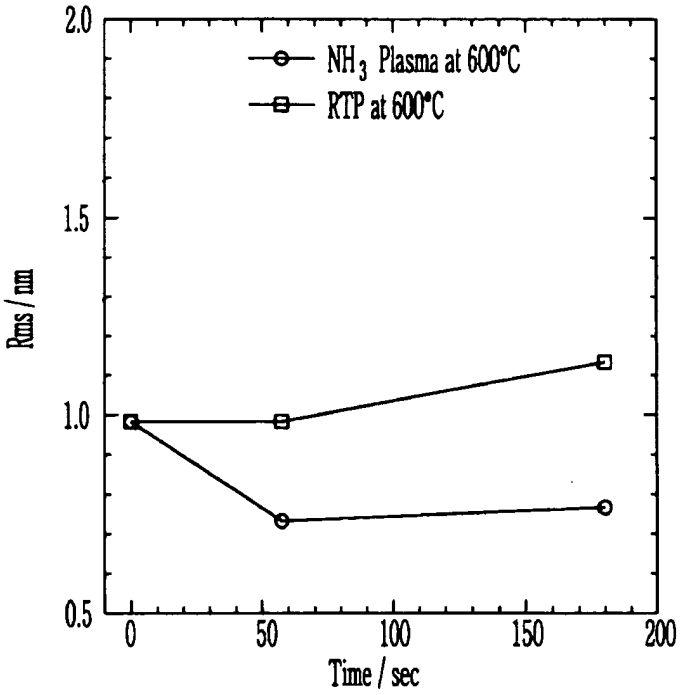
basis of a sidewall.

[Claim 13]

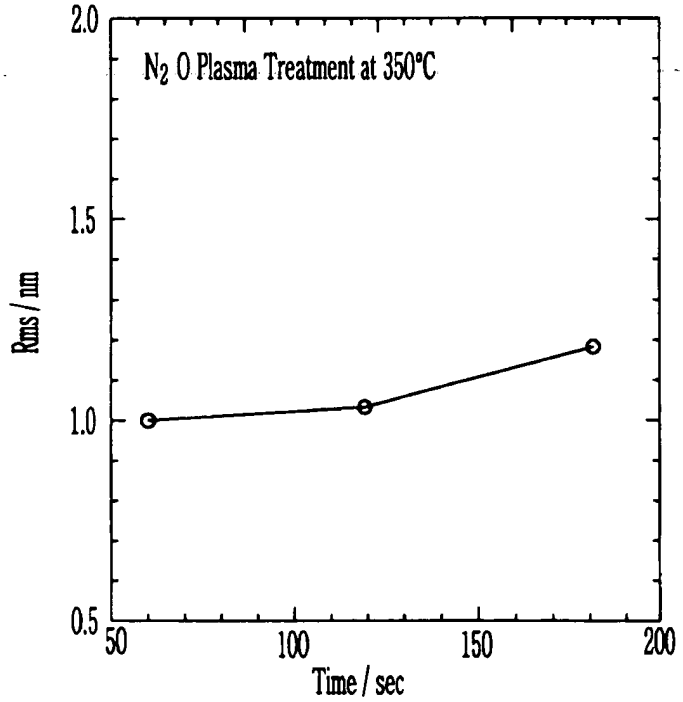
The method of manufacturing a capacitor in semiconductor devices according to claim 1, wherein in order to stabilize the entire capacitor structure in said seventh step, the capacitor structure is experienced by a thermal treatment using a mixture gas of oxygen and nitrogen or oxygen and argon at the temperature of 400-800□ for 1-130 minutes.

[DRAWINGS]

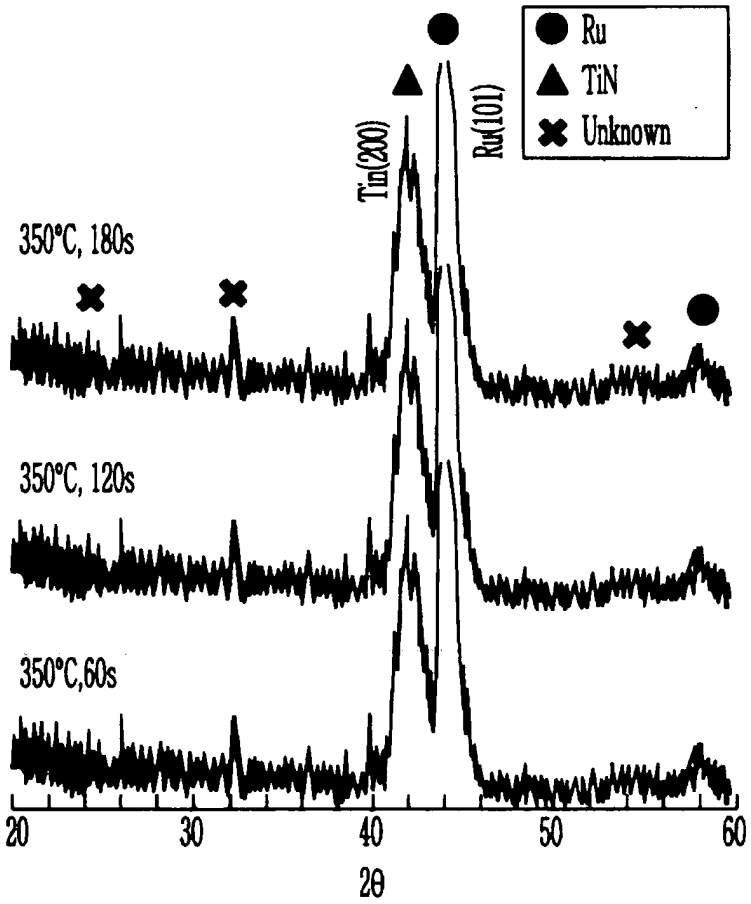
[FIG. 1]



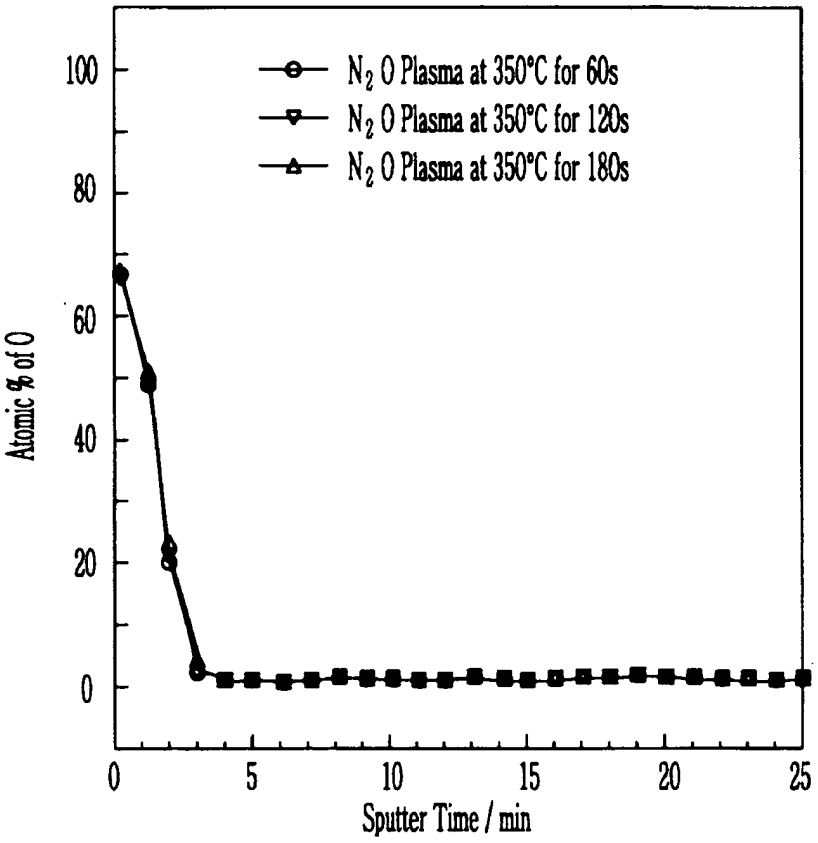
[FIG. 2]



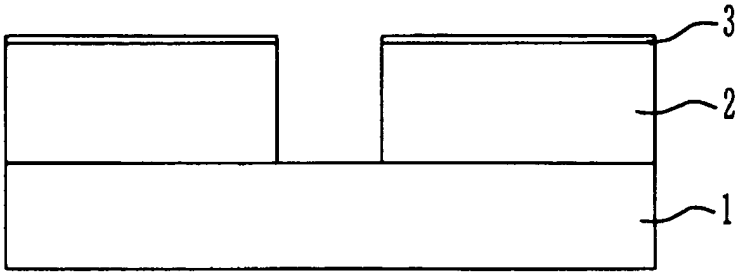
[FIG. 3]



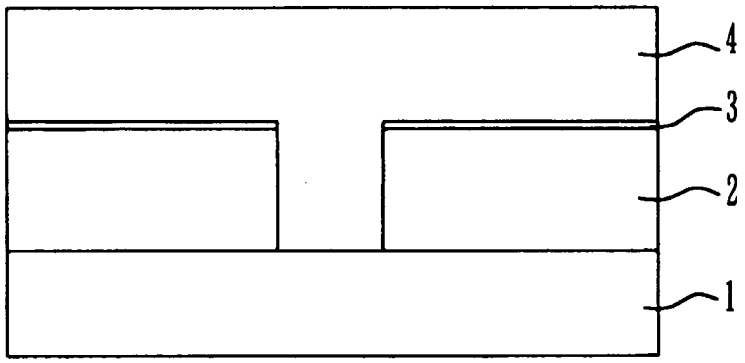
[FIG. 4]



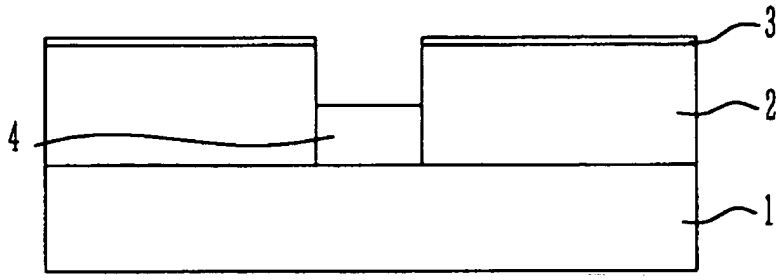
[FIG. 5]



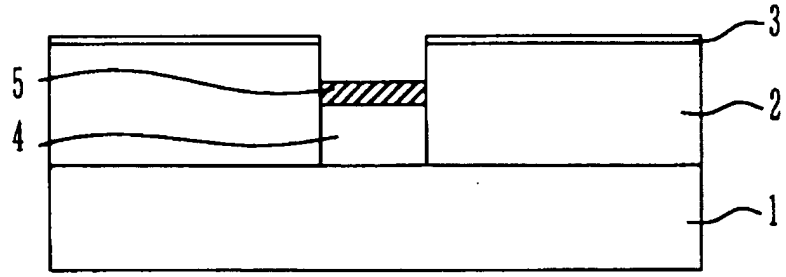
[FIG. 6]



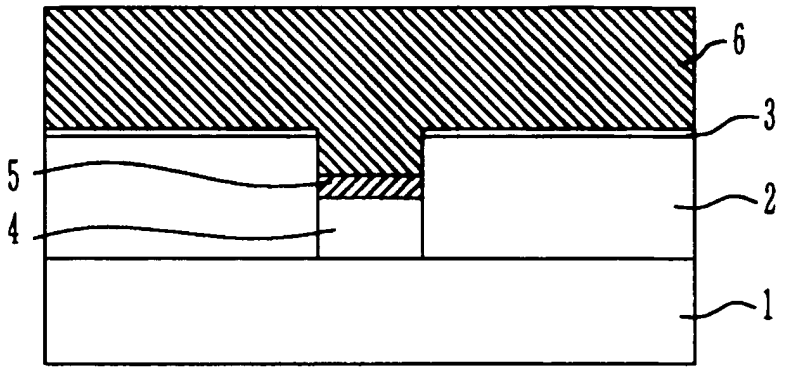
[FIG. 7]



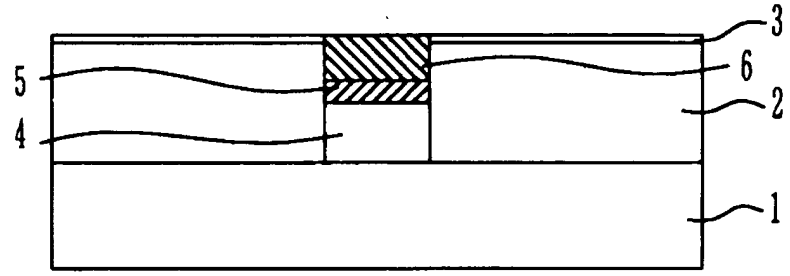
[FIG. 8]



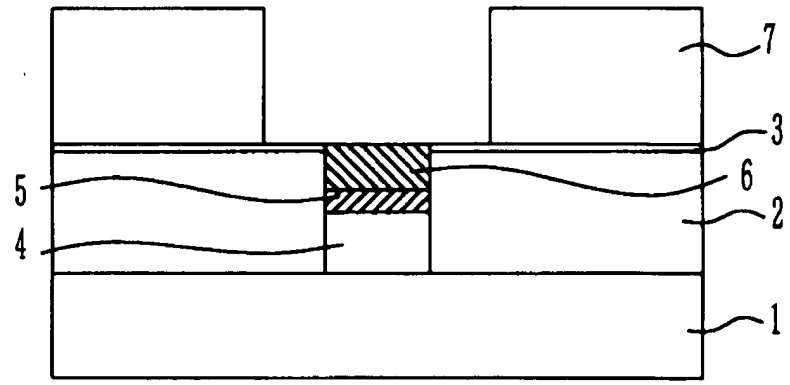
[FIG. 9]



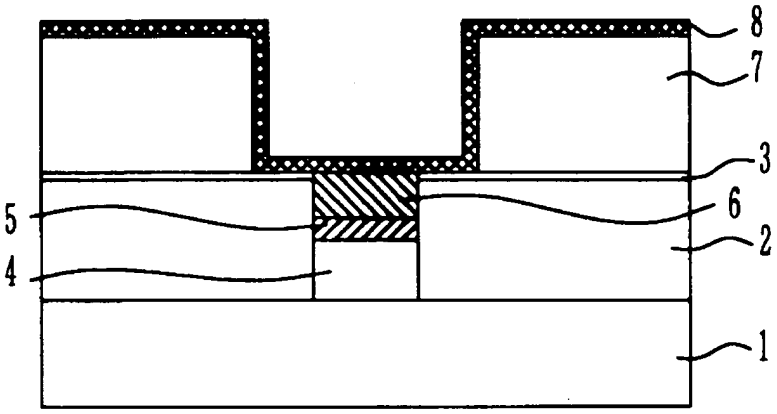
[FIG. 10]



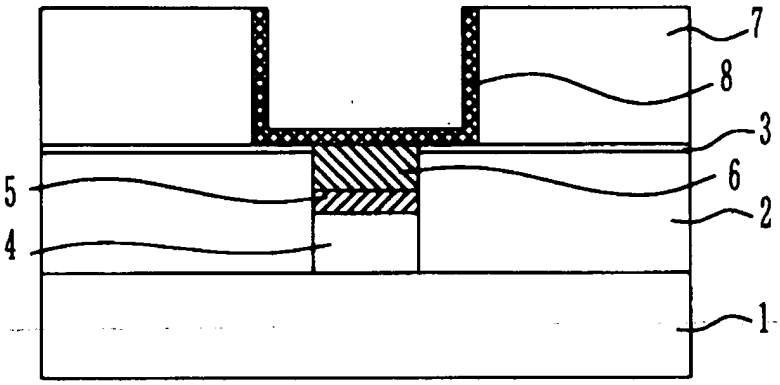
[FIG. 11]



[FIG. 12]



[FIG. 13]



[FIG. 14]